CSMSS

CHHATRAPATI SHAHU MAHARAJ SHIKSHAN SANSTHA's

CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE New Delhi, DTE (Govt. of Maharashtra) and affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere. Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 002 (M.S)

Ph. No. : (0240) 2646363, 2646350 Fax : (0240) 2379015

Email : shahuengg@gmail.com, principal@csmssengg.org Website : www.csmssengg.org

Date:- 26/10/2024

Department of Electronics Engineering (VLSI Design & Technology)

We are pleased to announce the Class Representative of Electronics Engineering (VLSI Design & Technology) department, academic year 2024-2025 for First Year and Second Year.

List of Class Representative

Sr No.	Class/Div	Roll Number	Name of the Student	CGPA/ HSC %	Mobile No.
1	First Year	VLSI 1121	SHEJUL TANVI SANDIP	88.17%	9021635998
2	Second Year	VLSI 2124	PERE SAKSHI KAKASAHEB	8.01	9529146642

C.S.M.S.S. Chh. Shahu College of Engineering Department of Electronics Engineering (VLSI Design & Technology) Kanchanwadi, Chh. Sambhajinagar (Aurangabad) M.S.

Dr. S. J. Honade

HoD

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Date: 28/11/2024

NOTICE

All the students of First Year B. Tech are hereby inform that they have to **enrol and register** for following respective NPTEL courses on website for upcoming semesters Jan-Apr 2025. Kindly share the enrolment and registration with the mentor on or before the 3rd Dec 2024.

Registration of NPTEL courses compulsory for First Year EE (VLSI D &T) students only

Sr. No	Name of resource person	Name of the institute offering the course	Course Name	Duration	Start Date	End Date	Enrolment Ends	Exam Registration Ends	Exam Date	SWYAM/NPTEL Course name and Web Link	Compulsory for Examination / Learning
01	Prof. Anupam Basu	IIT Kharagpur	Problem Solving Through Programming In C	12 weeks	20 Jan 2025	11 Apr 2025	27 Jan 2025	14 Feb 2025	27 Apr 2025 IST	https://onlinecourses.nptel.ac.in/noc25_cs56/preview	**Examination**

NPTEL Coordinator
Mr. G. G. Patil

Mentor

HOD
Dr. Shrikant J. Honade
Head of Department
Electronics Engineering
(VLSI Design & Technology)

C.S.M.S.S. Chh. Shahu College of Engineering ★ Kanchanwadi, Chh. Sambhajinagar (Aurangabad) M.S. ★
Department of Electronics Engineering (VLSI Design & Technology)

Principal
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Date: 28/11/2024

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Registration of NPTEL courses compulsory for Second Year EE (VLSI D &T) students only

Sr. No	Name of resource person	Name of the institute offering the course	Course Name	Duration	Start Date	End Date	Enrolment Ends	Exam Registration Ends	Exam Date	SWYAM/NPTEL Course name and Web Link	Compulsory for Examination / Learning
01	Prof. Shaik Rafi Ahamed	IIT Guwahati	Integrated Circuits and Applications	12 weeks	20 Jan 2025	11 Apr 2025	27 Jan 2025	14 Feb 2025	26 Apr 2025 IST	https://onlinecourses.nptel.ac.in/noc25_ee43/preview	**Examination**

NPTEL Coordinator
Mr. G.G. Patil

Mentor
Prof. T.A Momin

HOD
Dr. Shrikant J. Honade
Head of Department
Electronics Engineering
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Principal

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Email :shahuengg@gmail.com, principal@csmssengg.org Website : www.csmssengg.org
Department of Electronics Engineering (VLSI Design & Technology)

Date: - 07/11/2024

Selection List for Students Club EE VLSI (D&T) Engineering

Following is the list of students those who selected for various posts in VLSI students club from Electronics Engineering (VLSI D&T) Department for A.Y. 2024 Second Year.

Sr. No.	Post	Name of Member	Class
1	**Club President**	Rutuja Jagtap	Second Year
2	**Club Vice-President**	Sanket Nikam	Second Year
3	**Club Secretary**	Aditya Suryavanshi	Second Year
4	**Club Treasurer**	1. Aarya Kulkarni 2. Tanushri Sherkar	Second Year
5	**Event Coordinator**	Vaishnavi Shelke	Second Year
6	**Technical Lead (Electronics & Circuit Design)**	1. Nandinee Jadhav 2. Ashwini Divekar	Second Year
7	**Technical Lead (Coder)**	1. Pranav Rode 2. Vedashri Gavali	Second Year
8	**Public Relations Members (PRM)**	1. Avadhut Ude 2. Omkar Chavan 3. Prem Pawar	Second Year

Interview Date: 05/11/2024

Panel Members:

1) Dr. S. J. Honade
2) Dr. J. R. Shinde
3) Prof. T. A. Mohije
4) Prof. P. R. Bhusari
5) Prof. T. Y. Deshmukh
6) Prof. I. M. Palkar

Prof. G. G. Patil
Club Coordinator

C.S.M.S.S. Chh. Shahu College of Engineering
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HoD, EE (VLSI D &T)
Dr. Shrikant J. Honade
Head of Department
Electronics Engineering
(VLSI Design & Technology)

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Approved by AICTE New Delhi, DTE (Govt. of Maharashtra) and affiliated to Dr. BATU, Lonere (Raigad). DTE Code: 2533

ELECTRONICS ENGINEERING (VLSI D&T) DEPARTMENT

Date:-23/10/2024

Selection List

"Students Association of VLSI (D & T) Engineer's – SAVE"

Following is the list of students those who selected for various posts in VLSI Students Association (VISA) from Electronics Engineering (VLS D&T) Department for A.Y. 2024 Second Year.

Sr. No.	Post	Name of VISA Member	Class
01	President	DEVIKA RAVINDRA BODKHE	Second Year
02	Vice president	VAISHNAVI BALASAHEB SHELKE	Second Year
03	Treasurer	1. RUTUJA NILESH MAKARIYE 2. RAJNANDINI SATISH PATIL	Second Year
04	Event Manager	1. RUSHIKESH ANIL GAVHANE 2. SHEETAL SANTOSH ADHANE	Second Year
05	Ladies Representative	1. GAYATRI SUDHIR SHINDE	Second Year
06	Sports Coordinator	1. VIVEK NARAYAN BAMBARDE 2. SANKET BHIMRAV NIKAM	Second Year
07	Event coordinator	1. TANUSHRI SANTOSH SHERKAR 2. RADHIKA ARUN THORKAR 3. RUTUJA NARAYAN JAGTAP	Second Year
08	VISA Representative/ VISA Coordinator	1. VEDIKA SURAJ PATIL 2. BHAKTI JAGADISH SONWANE	Second Year
09	Media & Publicity	1. PREM DNYANESHWAR PAWAR	Second Year

Date of Conduct of Interview for **"SAVE 2024"**:- 10/10/2024

Panel Members: - 1) Dr. S. J. Honade
2) Dr. J. R. Shinde
3) Prof. T. A. Mohije
4) Prof. G. G. Patil
5) Prof. T. Y. Deshmukh
6) Prof. I. M. Palkar

Prof. P. R. Bhusari
Dept. VISA Coordinator

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Dr. S. J. Honade
HOD

Dr. Shrikant J. Honade
Head of Department
Electronics Engineering
(VLSI Design & Technology)