



CSMSS

CHHATRAPATI SHAHU MAHARAJ SHIKSHAN SANSTHA's

CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE New Delhi, DTE (Govt. of Maharashtra) and affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere. Kanchanwadi, Paithan Road, Chhatrapati Sambhajnagar 431 011 (M.S)

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Date: 10-03-2026

NOTICE

All the students of SE & TE -EE (VLSI D&T) are hereby informed that Class Test-I (CT-I) & Open Book Test – I (OBT-I) for Academic Year 2025-26(Even Semester) is scheduled as follows:

Open Book Test – I (OBT-I) : 11/03/2026 to 17/03/2026.

Class Test-I (CT-I): 12/03/2026 to 18/03/2026.

Note: Attendance is mandatory for all students during CT-I and OBT-I.

Detailed Timetable is displayed on Notice Board.



S. J. Honade
10/03/2026

Dr. S. J. Honade
HOD EE (VLSI D & T)

RMC - *[Signature]*
APS - *[Signature]*
PAK - *[Signature]*
TM - *[Signature]*
HGA - *[Signature]*
GAP - *[Signature]*
JOS - *[Signature]*



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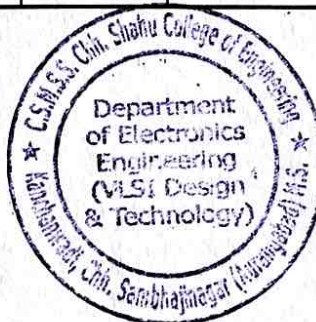
DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


CLASS TEST-I

Seating Arrangment

Sr No	Date	Time	Division	Hall No	Roll No	Subject
1	12.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Analog Circuits
			TE		VL3101-VL3136	Internet of Things & Industry 4.0
SE			209	VL2137-VL2172	Analog Circuits	
TE				VL3137-VL3174	Internet of Things & Industry 4.0	
3	13.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Network Theory & Signals and Systems
			TE		VL3101-VL3136	Digital VLSI Design
SE			209	VL2137-VL2172	Network Theory & Signals and Systems	
TE				VL3137-VL3174	Digital VLSI Design	
5	14.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Data Analytics
			TE		VL3101-VL3136	Semiconductor Materials Synthesis and Characterization/ Computer Networks
SE			209	VL2137-VL2172	Data Analytics	
TE				VL3137-VL3174	Semiconductor Materials Synthesis and Characterization/ Computer Networks	
7	16.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Patents and IPR
			TE		VL3101-VL3136	Artificial Intelligence & Machine Learning / Cloud Computing
SE			209	VL2137-VL2172	Patents and IPR	
TE				VL3137-VL3174	Artificial Intelligence & Machine Learning / Cloud Computing	
9	17.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Marathi
			TE		VL3101-VL3136	Employability and Skill Development
SE			209	VL2137-VL2172	Marathi	
TE				VL3137-VL3174	Employability and Skill Development	
11	18.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	System Design using Verilog
				301	VL2137-VL2172	System Design using Verilog
11	20.03.2026	10.30AM TO 11.00AM	SE	208	VL2101-VL2136	Educational Leadership
				301	VL2137-VL2172	Educational Leadership


Prof. P.N.Kathar
CLASS TEST CO-ORDINATOR




Dr. S.U. Honade
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CLASS TEST-I TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	12.03.2026	10:30 AM to 11:00 AM	SE	Analog Circuits
2	13.03.2026	10:30 AM to 11:00 AM	SE	Network Theory & Signals and Systems
3	14.03.2026	10:30 AM to 11:00 AM	SE	Data Analytics
4	16.03.2026	10:30 AM to 11:00 AM	SE	Patents and IPR
5	17.03.2026	10:30 AM to 11:00 AM	SE	Marathi
6	18.03.2026	10:30 AM to 11:00 AM	SE	System Design using Verilog
7	20.03.2026	10:30 AM to 11:00 AM	SE	Educational Leadership


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OPEN BOOK TEST - I

TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	11.03.2026	04:15PM to 05:15PM	SE	Analog Circuits
2	12.03.2026	04:15PM to 05:15PM	SE	Network Theory & Signals and Systems
3	13.03.2026	04:15PM to 05:15PM	SE	Data Analytics
4	14.03.2026	04:15PM to 05:15PM	SE	Patents and IPR
5	16.03.2026	04:15PM to 05:15PM	SE	Marathi
6	17.03.2026	04:15PM to 05:15PM	SE	System Design using Verilog
7	18.03.2026	04:15PM to 05:15PM	SE	Educational Leadership


Prof. P.N. Kathar
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**CLASS TEST-I
TIME TABLE**

Sr. No.	Date	Time	Class	Subject
1	12.03.2026	10:30AM to 11:00AM	TE	Internet of Things & Industry 4.0
2	13.03.2026	10:30AM to 11:00AM	TE	Digital VLSI Design
3	14.03.2026	10:30AM to 11:00AM	TE	Semiconductor Materials Synthesis and Characterization / Computer Networks
4	16.03.2026	10:30AM to 11:00AM	TE	Artificial Intelligence & Machine Learning / Cloud Computing
5	17.03.2026	10:30AM to 11:00AM	TE	Employability and Skill Development


Prof. P.N.Kathar

CLASS TEST CO-ORDINATOR



Dr. S. J. Honade

HOD

