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# CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,  
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.




## DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)

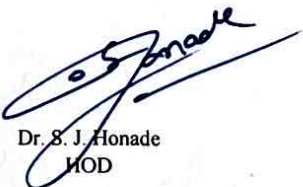
### CLASS TEST-II

#### Seating Arrangment

Sr No	Date	Time	Division	Hall No	Roll No	Subject
1	10.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Engineering Mathematics –III
			TE		VL3101-VL3135	Introduction to VLSI Life Cycle & Micro-fabrication
2	10.11.2025	10.30AM TO 11.00AM	SE	209	VL2136-VL2167	Engineering Mathematics –III
			TE		VL3136-VL3168	Introduction to VLSI Life Cycle & Micro-fabrication
3	11.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Electronics Devices & Circuits
			TE		VL3101-VL3135	Microcontroller & Embedded System
4	11.11.2025	10.30AM TO 11.00AM	SE	209	VL2136-VL2167	Electronics Devices & Circuits
			TE		VL3136-VL3168	Microcontroller & Embedded System
5	12.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Digital System Design & Microprocessor
			TE		VL3101-VL3135	Control System Engineering / Semiconductor Device Modeling
6	12.11.2025	10.30AM TO 11.00AM	SE	209	VL2136-VL2167	Digital System Design & Microprocessor
			TE		VL3136-VL3168	Control System Engineering / Semiconductor Device Modeling
7	13.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Open Elective -SSD
			TE		VL3101-VL3135	Database Management Systems / Java Programming
8	13.11.2025	10.30AM TO 11.00AM	SE	209	VL2136-VL2167	Open Elective -SSD
			TE		VL3136-VL3168	Database Management Systems / Java Programming
9	14.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Universal Human Values II
			TE		VL3101-VL3135	Project Management
10	14.11.2025	10.30AM TO 11.00AM	SE	209	VL2136-VL2167	Universal Human Values II
			TE		VL3136-VL3168	Project Management
11	15.11.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2135	Employability and Skill Development
				301	VL3101-VL3135	Employability and Skill Development
12	17.11.2025	10.30AM TO 11.00AM	SE	208	VL2136-VL2167	MDM
				301	VL3136-VL3168	MDM

  
Prof. P.N. Kathar  
CLASS TEST CO-ORDINATOR



  
Dr. S. J. Honade  
MOD



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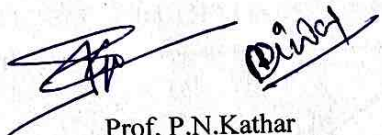
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## DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T) OPEN BOOK TEST - III TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	08.11.2025	04:15PM to 05:15PM	TE	Introduction to VLSI Life Cycle & Micro-fabrication
2	10.11.2025	04:15PM to 05:15PM	TE	Microcontroller & Embedded System
3	11.11.2025	04:15PM to 05:15PM	TE	Control System Engineering / Semiconductor Device Modeling
4	12.11.2025	04:15PM to 05:15PM	TE	Database Management Systems / Java Programming
5	13.11.2025	04:15PM to 05:15PM	TE	Project Management

  
Prof. P.N.Kathar  
CLASS TEST CO-ORDINATOR



  
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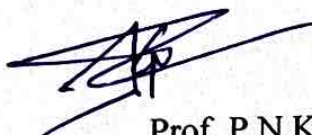


## DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


### OPEN BOOK TEST - III

### TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	08.11.2025	04:15PM to 05:15PM	SE	Engineering Mathematics –III
2	10.11.2025	04:15PM to 05:15PM	SE	Electronics Devices & Circuits
3	11.11.2025	04:15PM to 05:15PM	SE	Digital System Design & Microprocessor
4	12.11.2025	04:15PM to 05:15PM	SE	Open Elective-SSD
5	13.11.2025	04:15PM to 05:15PM	SE	Universal Human Values II
6	14.11.2025	04:15PM to 05:15PM	SE	Employability and Skill Development
7	15.11.2025	04:15PM to 05:15PM	SE	MDM

  
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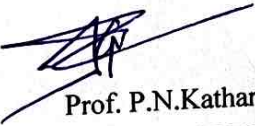


### DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


#### CLASS TEST-II

#### TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	10.11.2025	10:30 AM to 11:00 AM	SE	Engineering Mathematics –III
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