



CSMSS

## CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,  
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.




### DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


### OPEN BOOK TEST - II (MSE)

#### TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	01.10.2025	03:15 PM to 05:15 PM	SE	Digital System Design & Microprocessor
2	03.10.2025	03:15 PM to 05:15 PM	SE	Electronics Devices & Circuits
3	04.10.2025	03:15 PM to 05:15 PM	SE	Engineering Mathematics -III
4	06.10.2025	03:15 PM to 05:15 PM	SE	Open Elective -SSD
5	07.10.2025	03:15 PM to 05:15 PM	SE	MDM-Python Programing
6	08.10.2025	03:15 PM to 05:15 PM	SE	Employability and Skill Development
7	09.10.2025	03:15 PM to 05:15 PM	SE	Universal Human Values II

  
Prof. P.N.Kathar  
CLASS TEST CO-ORDINATOR



  
Dr. S. J. Honade  
HOD



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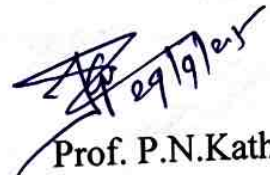
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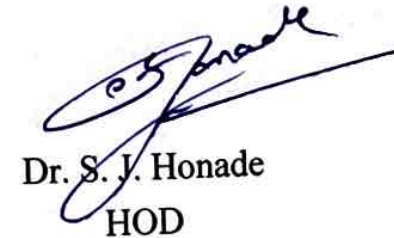
### MID\_SEM EXAM TIME TABLE TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	03.10.2025	10:15AM to 11:15AM	SE	Digital System Design & Microprocessor
2	04.10.2025	10:15AM to 11:15AM	SE	Electronics Devices & Circuits
3	06.10.2025	10:15AM to 11:15AM	SE	Engineering Mathematics -III
4	07.10.2025	10:15AM to 11:15AM	SE	Open Elective -SSD
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Sr. No.	Date	Time	Class	Subject
1	03.10.2025	10:15AM to 11:15AM	TE	Introduction to VLSI Life Cycle & Micro-fabrication
2	04.10.2025	10:15AM to 11:15AM	TE	Microcontroller & Embedded System
3	06.10.2025	10:15AM to 11:15AM	TE	Control System Engineering / Semiconductor Device Modeling
4	07.10.2025	10:15AM to 11:15AM	TE	Database Management Systems / Java Programming
5	08.10.2025	10:15AM to 11:15AM	TE	Project Management

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### OPEN BOOK TEST - II(MSE)

#### TIME TABLE

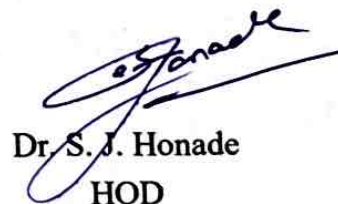
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29/9/25

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