

CSMSS
CHIL SHAHU COLLEGE OF ENGINEERING
KANCHANWADI, CHILSAMBHAJINAGAR -431002

DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)

3RD SEMESTER CLASS TEST-I RESULT SUMMARY

Sr No	Total Students	No of Students
1	Passed students in All Subjects	42
2	Fail Students in 5 Subject	0
3	Fail Students in 4 Subject	2
4	Fail Students in 3 Subject	2
5	Fail Students in 2 Subject	9
6	Fail Students in 1 Subject	8
7	Total No of Students	63
8	% of All Clear passing	61.76


Prof. P. N. Kathar
Exam Coordinator


Dr. S. J. Honade
HOD



CSMSS

CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.




DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


CLASS TEST-I

Seating Arrangement

Sr No	Date	Time	Division	Hall No	Roll No	Subject
1	02.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Engineering Mathematics -III
			TE	208	VL3101-VL3174	Introduction to VLSI Life Cycle & Micro-fabrication
2	02.09.2025	10.30AM TO 11.00AM	SE	209	VL2131-VL2161	Engineering Mathematics -III
			TE	209	VL3136-VL3174	Introduction to VLSI Life Cycle & Micro-fabrication
3	03.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Electronics Devices & Circuits
			TE	208	VL3101-VL3174	Microcontroller & Embedded System
4	03.09.2025	10.30AM TO 11.00AM	SE	209	VL2131-VL2161	Electronics Devices & Circuits
			TE	209	VL3136-VL3174	Microcontroller & Embedded System
5	04.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Digital System Design & Microprocessor
			TE	208	VL3101-VL3174	Control System Engineering / Semiconductor Device Modeling
6	04.09.2025	10.30AM TO 11.00AM	SE	209	VL2131-VL2161	Digital System Design & Microprocessor
			TE	209	VL3136-VL3174	Control System Engineering / Semiconductor Device Modeling
7	08.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Open Elective
			TE	208	VL3101-VL3174	Database Management Systems / Java Programming
8	08.09.2025	10.30AM TO 11.00AM	SE	209	VL2131-VL2161	Open Elective
			TE	209	VL3136-VL3174	Database Management Systems / Java Programming
9	09.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Universal Human Values II
			TE	208	VL3101-VL3174	Project Management
10	09.09.2025	10.30AM TO 11.00AM	SE	209	VL2131-VL2161	Universal Human Values II
			TE	209	VL3136-VL3174	Project Management
11	10.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	MDM
				301	VL2131-VL2161	MDM
12	11.09.2025	10.30AM TO 11.00AM	SE	208	VL2101-VL2130	Employability and Skill Development
				301	VL2131-VL2161	Employability and Skill Development


Prof. P.N. Kathar
CLASS TEST CO-ORDINATOR




Dr. S. J. Honade
HOD



CSMSS


CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.




DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T) OPEN BOOK TEST - I TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	30.08.2025	04:15PM to 05:15PM	SE	Engineering Mathematics –III
2	02.09.2025	04:15PM to 05:15PM	SE	Electronics Devices & Circuits
3	03.09.2025	04:15PM to 05:15PM	SE	Digital System Design & Microprocessor
4	04.09.2025	04:15PM to 05:15PM	SE	Open Elective
5	08.09.2025	04:15PM to 05:15PM	SE	Universal Human Values II
6	09.09.2025	04:15PM to 05:15PM	SE	MDM
7	10.09.2025	04:15PM to 05:15PM	SE	Employability and Skill Development


Prof. P.N.Kathar

CLASS TEST CO-ORDINATOR




Dr. S. J. Honade
HOD



CSMSS

CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.



DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)

CLASS TEST-I

TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	02.09.2025	10:30 AM to 11:00 AM	SE	Engineering Mathematics –III
2	03.09.2025	10:30 AM to 11:00 AM	SE	Electronics Devices & Circuits
3	04.09.2025	10:30 AM to 11:00 AM	SE	Digital System Design & Microprocessor
4	08.09.2025	10:30 AM to 11:00 AM	SE	Open Elective
5	09.09.2025	10:30 AM to 11:00 AM	SE	Universal Human Values II
6	10.09.2025	10:30 AM to 11:00 AM	SE	MDM
7	10.09.2025	10:30 AM to 11:00 AM	SE	Employability and Skill Development

Prof. P.N.Kathar

CLASS TEST CO-ORDINATOR



Dr. S. J. Honade

HOD



CSMSS

CHH. SHAHU COLLEGE OF ENGINEERING

Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.



DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T) OPEN BOOK TEST - I

TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	30.08.2025	04:15PM to 05:15PM	TE	Introduction to VLSI Life Cycle & Micro-fabrication
2	02.09.2025	04:15PM to 05:15PM	TE	Microcontroller & Embedded System
3	03.09.2025	04:15PM to 05:15PM	TE	Control System Engineering / Semiconductor Device Modeling
4	04.09.2025	04:15PM to 05:15PM	TE	Database Management Systems / Java Programming
5	08.09.2025	04:15PM to 05:15PM	TE	Project Management

Prof. P.N.Kathar
CLASS TEST CO-ORDINATOR



Dr. S. J. Honade
HOD



CSMSS

CHH. SHAHU COLLEGE OF ENGINEERING


Approved by AICTE-New Delhi, DTE-Govt. of Maharashtra,
Affiliated to Dr. Babasaheb Ambedkar Technological University, Lonere.



DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI D&T)


CLASS TEST-I TIME TABLE

Sr. No.	Date	Time	Class	Subject
1	02.09.2025	10:30AM to 11:00AM	TE	Introduction to VLSI Life Cycle & Micro-fabrication
2	03.09.2025	10:30AM to 11:00AM	TE	Microcontroller & Embedded System
3	04.09.2025	10:30AM to 11:00AM	TE	Control System Engineering / Semiconductor Device Modeling
4	08.09.2025	10:30AM to 11:00AM	TE	Database Management Systems / Java Programming
5	09.09.2025	10:30AM to 11:00AM	TE	Project Management


Prof. P.N.Kathar

CLASS TEST CO-ORDINATOR




Dr. S. J. Honade
HOD