Schedule of BASIC FDP

FDP Application Number: 1716464999

Title of the FDP: Semiconductor Design & Its Integration with Disruptive Technological Innovations

FDP Start Date: 9/09/2024 **FDP End Date:** 14/09/2024

Day 1	Day 2	Day 3	Day 4	Day 5	Day 6
9:00 – 9:30 **Inauguration**					
9:30 – 12:00 **Session 1** 1. **Name of the Expert:** Dr. *Vadthiya Narendar* 2. **Designation:** *Assistant Professor* 3. **Organization:** *NIT Warangal, Telangana* 4. **Experience in Years:** *10 Years* 5. **Topic to be taught:** *VLSI & Nanoelectronics*	**9:30 – 12:00** **Session 3** 1. **Name of the Expert:** Dr. Gajanan Awari 2. **Designation:** Professor & AICTE Nominated Margdarshak and Chief Coordinator 3. **Organization**: Government Polytechnic, Nagpur, MS 4. **Experience in Years:** 25 Years 5. **Topic to be taught:** Semiconductors Integration in Electric Vehicles	**9:30 – 12:00** **Session 5** 1. **Name of the Expert:** *Mr. RajVardhan* 2. **Designation:** *Technical Director* 3. **Organization:** *JDMTech Semiconductor Pvt Ltd* 4. **Experience in Years:** *16 years* 5. **Topic to be taught:** *AI implementation in Design for Testability*	**9:30 – 12:00** **Session 7** 1. **Name of the Expert:** *Dr. Jitesh Shinde* 2. **Designation:** *Associate Professor* 3. **Organization:** CSMSS Chh. Shahu College of Engineering, Chh. Sambhajinagar 4. **Experience in Years:** *16 years* 5. **Topic to be taught:** *NEP2020 for Semiconductor-Based Curriculum*	**9:00 – 1:00** **Industrial visit** 1. **Name of the Organization:** *National Institute of Electronics & Information Technology* 2. **Complete address with pincode :** *Dr. B.A, M. University Campus, Dr Babasaheb Ambedkar Marathwada University Campus, Aurangabad, Maharashtra 431004* 3. **Industry Type:** *Electronics & Information Technology* 4. **Area of specification:** *Electronics, IT and knowledge-based enterprise*	**9:30 – 12:00** **Session 10** 1. **Name of the Expert:** *Dr. M. Krishnasamy* 2. **Designation:** *Assistant Professor, Senior Grade-2* 3. **Organization:** *Vellore Institute of Technology (VIT-AP University), Amravathi, Andhra Pradesh* 4. **Experience in Years:** *14 years* 5. **Topic to be taught:** *MEMS Device Design, Renewable Energy Systems and Microelectronics*
12:00 – 1:00 **Article Discussion** **1.Title of the Research Paper:** *Implementation of deep neural networks on FPGA-CPU platform using Xilinx SDSOC* **2. Name of the journal:** *Analog Integrated Circuits and Signal Processing* **3. Year of Publication:** *2020*	**12:00 – 1:00** **Article Discussion** **1.Title of the Research Paper:** *Yield constrained automated design algorithm for power optimized pipeline ADC* **2. Name of the journal:** *Integration, the VLSI Journal* **3. Year of Publication:** *2020*	**12:00 – 1:00** **Article Discussion** **1.Title of the Research Paper:** *A 7.5 Gb/s/pin 8-Gb LPDDR5 SDRAM with Various High-Speed and Low-Power Techniques* **2. Name of the journal:** *IEEE Journal of Solid-State Circuits* **3. Year of Publication:** *2020*	**12:00 – 1:00** **Article Discussion** **1.Title of the Research Paper:** *10-to-112-Gb/s DSP –DAC-Based Transmitter in 7 nm FinFET with Flex Clocking Architecture* **2. Name of the journal:** *IEEE Journal of Solid-State Circuits* **3. Year of Publication:** *2021*		**12:00 – 1:00** **Article Summary**
1:00 – 2:00 **Lunch**	**1:00 – 2:00** **Lunch**	**1:00 – 2:00** **Lunch**	**1:00 – 2:00** **Lunch**	**1:00 – 2:00** **Lunch**	**1:00 – 2:00** **Lunch**
2:00 – 4:30 **Session 2** 1. **Name of the Expert:** Dr. *Vadthiya Narendar* 2. **Designation:** *Assistant Professor* 3. **Organization:** *NIT Warangal, Telangana* 4. **Experience in Years:** *10 Years* 5. **Topic to be taught:** *VLSI & Nanoelectronics with Practical Approach*	**2:00 – 4:30** **Session 4** 1. **Name of the Expert:** Mr. Shrikant Atkarne 2. **Designation:** Head Technical 3. **Organization:** Spaarta Soft Technology Solutionss, Pune 4. **Experience in Years:** 15 years 5. **Topic to be taught:** Next Generation Nano Electronics Devices Circuits and its Application using EDA Simulation Tools	**2:00 – 4:30** **Session 6** 1. **Name of the Expert:** *Mr. RajVardhan* 2. **Designation:** *Technical Director* 3. **Organization:** *JDMTech Semiconductor Pvt Ltd* 4. **Experience in Years:** *16 years* 5. **Topic to be taught:** *Semiconductor integration with Machine Learning*	**2:00 – 4:30** **Session 8** 1. **Name of the Expert:** *Dr. Jayaraj U. Kidav* 2. **Designation:** *Executive Director* 3. **Organization:** *National Institute of Electronics & Information Technology* 4. **Experience in Years:** *15 years* 5. **Topic to be taught:** *ASIC Physical Design*	**2:00 – 4:30** **Session 9** 1. **Name of the Expert:** Mr. Ashish Suresh Khachane 2. **Designation:** Interface IP Application Engineer 3. **Organization:** Intel India 4. **Experience in Years:** 12 years 5. **Topic to be taught:** Recent Trends in Semiconductor integration in disruptive technologies	**2:00 – 4:00** **MCQ & Reflection Journal**
4:30 – 5:30 **Hands-on training /Labs preferably using FOSS tools**	**4:30 – 5:30** **Hands-on training /Labs preferably using FOSS tools**	**4:30 – 5:30** **Hands-on training /Labs preferably using FOSS tools**	**4:30 – 5:30** **Hands-on training /Labs preferably using FOSS tools**	**4:30 – 5:30** **Hands-on training /Labs preferably using FOSS tools**	**4:00 – 5:00** **Valedictory Session**