CSMSS
CHH. SHAHU COLLEGE OF ENGINEERING
Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar (Aurangabad) 431 011 (M.S)

Department of Electronics and Communication
(Advanced Communication Technology)

FORM NO.	AC-07A
REV. NO. ISSUE DATE	00, December 2024

E&C(ACT)		CLASS TIME TABLE		CLASS	Second Year
ACADEMIC YEAR:	2025-26	SEMESTER:	EVEN	CLASS ROOM NO.	B-604
				W.E.F.	29.12.2025

Time	10:15AM to 11:15AM	11:15AM to 12:15PM	12:15 to 01:00	01:00PM to 02:00PM	02:00PM to 03:00PM	03:00 to 03:15	03:15PM to 04:15PM	04:15PM to 05:15PM
	1	2		3	4		5	6
MON	MP	MDM (DA)		COI	NA		NA (S1) / ADC (S2) / MP (S3)	
TUE	OEL(EL)	MAR		NA	ADC		NA (S3) / ADC (S1) / MP (S2)	
WED	ADC	MP		IPR	MDM (DA)		NA	OEL(EL)
THU	PCB (S2) / DA (S1)			MDM (DA)	OEL(EL)		MP	LODBA
FRI	NA	IPR		NA (S2)-SHJ/ADC (S3) / MP (S1)			ADC	LIB/TG MEET/NPTEL/SPORT
SAT	MP	ADC		PCB (S1) / DA (S2)			COI	MAR

Subject Name	Faculty Name
Network Analysis (NA)	Prof. S. H. Jadhav
Microprocessors (MP)	Prof. A.R.Palaskar
OEL (Educational Leadership)/ADC (Analog & Digital Communication)	Prof. V.L.Nagre
Data Analyist (MDM) DA	Prof. A. T. Jadhav
Constitution of India (COI)	Prof. S. R. Kadam
Patent & IPR (IPR)	Prof. A. M. Kadli
Marathi (MAR)	Prof. A. G. Gaikwad

Practical Lab	Faculty Name	Lab No
Network Analysis	Prof. S. H. Jadhav	B-602
Analog and Digital Communication	Prof. V.L.Nagre	B-603
Microprocessors	Prof. A.R.Palaskar	B-609
Data Analyist (MDM)	Prof. A. T. Jadhav	B-515
Printed Circuit Board Design	Prof. A. M. Kadli	B-502

BATCHES	
BATCH: S 1	2101 TO 2125
BATCH: S 2	2126 TO 2150
BATCH: S 3	2151 TO 2174

Practical/ Lab	BATCH
Data Analyist (MDM)	(S1)2101-2136 &(S2) 2137-2174
PCB Design	(S1)2101-2136 &(S2) 2137-2174

CLASS TEACHER	Prof. A. R. Palaskar
TG: S 1	Prof. S. H. Jadhav
TG: S 2	Prof. A. R. Palaskar
TG: S 3	Prof. A. T. Jadhav

Time Table Cordinator

Academic Coordinator

HOD 29/12/25

Dean Academics

Principal